What is claimed is:

1. A system for addressing a data storage unit used in at least one of server and client computers, which comprises:

means for converting an external bus into an internal bus for use in the system;

a memory module for storing data on the internal bus therein, the memory module being divided into a plurality of equally-sized memory blocks; and

means for processing writing data on the internal bus in the memory module and reading out the data therefrom.

2. The system of claim 1, wherein the internal bus is a PCI (Peripheral Component Interconnect Bus) interface bus

3. The system of claim 1, wherein the converting means includes a SCSI (Small Computer System Interface) interface bus.

4. The system of claim 1, wherein the memory module is composed of any one of SDRAM(Synchronous Dynamic Random Access Memory), rambus DRAM(Dynamic Random Access Memory), DDR(Double Data Rate) or other equivalent memories.

5. The system of claim 1, wherein each of the plurality of equally-sized memory blocks is divided into a predetermined number of equally-sized sub-memories.

6. The system of claim 1, wherein the predetermined number is four.

7. The system of claim 5, wherein the memory module employs a tree hierarchical configuration, which again compensates signals at an intermediate stage and forwards it to a lower hierarchy.

8. The system of claim 7, wherein the memory module includes a PCI to memory controller of a tree hierarchical configuration, which is disposed between the internal bus and the plurality of sub-memories as a bridge, for controlling access to the plurality of sub-memories, which are distributed in a hierarchical fashion.

9. The system of claim 8, wherein the tree hierarchical configuration is designed to allow a clock delay to be compensated at the PCI to memory controller.

10. The system of claim 4, wherein the PCI to memory controller activates any of the plurality of sub-

memories to be actually accessed and maintains the remaining in a low power mode.

11. The system of claim 10, wherein the PCI to memory controller includes a register block having a lower address bit, an upper address bit and a select bit, wherein the lower address bit represents an address of a set region within a memory map, which is in the range of the address region, the upper address bit is set when a memory address region from which the memory map is departed is used, and the select bit is used to directly access the memory module.